A WCDMA/HSDPA Baseband Processor

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***Abstract*— In this paper, a baseband processor including whole transceiver system for WCDMA/HSDPA communications is presented. In order to resist the non-ideal effect of the wireless channel, the receiver of the proposed processor consists of a channel estimator for channel estimation and receiver parameters calculation, a carrier frequency synchronization and timing synchronization block for carrier frequency offset and clock offset compensation, moreover, an adaptive equalizer for ISI suppression. In receiver architecture design, we adopt applicable algorithms to design each building blocks, so as to minimize the area complexity and power consumption but still with good performance. After system architecture design and system performance simulation, we do some rough evaluation from system architecture about the area and power consumption of the proposed processor.**

I. Introduction

Before 3G mobile communication systems, the most personal communication service is voice service limited by transmission data rate. However, in order to increase the transmission data rate further, 3GPP/WCDMA introduces **H**igh **S**peed **D**ownlink **P**acket **A**ccess (HSDPA) in Release 4 and 5 [1]–[5].

Since the higher modulation, higher coding rate, and more advance transmission techniques have adopted to achieve higher system transmission rate, it is a tendency towards system complexity increasing.

In this paper, a digital baseband processor for WCDMA/HSDPA communications systems with modified multiple-dwell detection method for multi-path searching, a frequency recovery loop to obtain fast carrier synchronization, a timing synchronization to provide correct data sampling, and finally a chip level equalizer to combat inter-symbol interference is proposed.

The rest of the paper is as follows. In section II, the HSDPA system is briefly. Transmitter, receiving techniques and system performance simulation are provided in section III and section IV respectively. Architecture analysis are presented in section V. Finally, some conclusions are given in section VI.

II. System Description

The system design specifications are listed in Table 1. The proposed baseband transceiver is designed to achieve highest data rate of 10 Mbps information bit rate of HS-PDSCH when the system reaches the maximum peak throughput under 16-QAM data modulation, 3/4 coding rate, and 15 multi-code transmitted simultaneously.

This research is supported in part by the National Science Council, Taiwan, R.O.C. under Grants NSC-94-2220-E-007-018 and National Chip Implementation Center.

TABLE I
Design Specification.

Physical channel	CPICH, HS-SCCH, HS-PDSCH
Modulation type	CPICH : QPSK HS-SCCH : QPSK HS-PDSCH : QPSK / 16-QAM
SF	CPICH : 256 (fixed) HS-SCCH : 128 (fixed) HS-PDSCH : 16 (fixed)
Detection	CPICH Coherent Detection
Chip rate	3.84 Mcps
Scrambling code	Complex Gold code sequence
Spreading code	Hadamard code
Multi-code transmission	Up to 15 multi-code transmission simultaneously

III. Architecture Design

A. Transmitter

There are mainly three incoming data in the transmitter before entering the complex scrambling for processing individual physical channel data symbols simultaneously. The data modulation for CPICH and HS-SCCH are QPSK. The data mapping of the HS-PDSCH has been adopted under QPSK, 16-QAM or even higher order modulation type in the future. There is an AMC functional block to handle the modulation type and the number of multi-code transmission channel via a serial to parallel device.

B. Receiver

The whole architecture of proposed transceiver system is shown in Fig. 1. The receiver can be separated into four parts: synchronization, equalization, de-spreading and symbol recovery.

C. Synchronization

The synchronization part consists of a channel estimator, carrier synchronization, and a timing synchronization.

In HSDPA systems, CPICH is the pilot channel with known pattern for estimating the wireless channel conditions when the receiver receives data. The data symbol from transmitter can be represented as:

$$S_{tx} = C_{sp}(S_{MI} + jS_{MQ}) * (C_{scI} + jC_{scQ}), \quad (1)$$

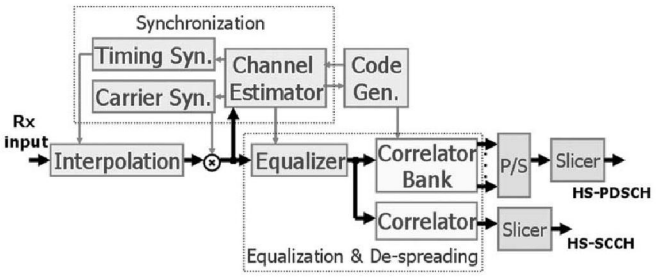

Fig. 1. Block diagram of the receiver.

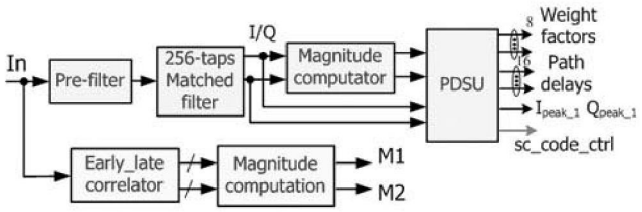

Fig. 2. Block diagram of channel estimator.

where S_{MI} and S_{MQ} are the I/Q channel symbols consist of pilot and data information, the spreading code is notated as C_{sp} and $C_{sc} = (C_{scI} + jC_{scQ})$ is the complex scrambling code. The pilot symbol extraction in receiver can be shown as:

$$S_{rx\_CPICH}(n) = S_{tx}(n)C_{sp\_CPICH}(n) * C_{sc}(n)^*, \tag{2}$$

where $S_{sp\_CPICH}(n)$ is the corresponding spreading code of the CPICH. After removing the spreading code of CPICH and scrambling code, I/Q values of the received pilot symbols can be re-written as:

$$\begin{aligned} &S_{rx\_CPICH}(n) \\ &= \sum_{n=1}^{256} 2C_{sp\_CPICH}(n)C_{sp\_CPICH}(n)(S_{MI} + jS_{MQ}), \\ &= 2 \times 256(S_{MI} + jS_{MQ}). \end{aligned} \tag{3}$$

A matched filter is commonly chosen in the channel estimator for fast and parallel correlation [6]. However, a symbol length matched filter may cause huge area overhead. Especially, the spreading factor of the CPICH is 256. Therefore, a pilot symbol length matched filter is unacceptable. In the proposed receiver, the multiple-dwell searching algorithm [7] is adopted which can save large area cost without losing the system performance seriously. Certainly, it can also reduce the power consumption efficiently. Fig. 2 is the block diagram of proposed channel estimator. It consists of a pre-filter, a complex-valued matched filter, a magnitude computation unit, an algorithm control unit and an early-late correlator. Since the multiple-dwell detection algorithm is adopted with 4 detection steps, we just need a 1/4 pilot symbol length matched filter $(256(taps) = 64(chips) * 4(oversampling))$ to collect the data symbols from the pre-filter and calculate the segmental correlations. The **p**ath **d**etection and **s**earching **u**nit (PDSU) executes the multiple-dwell detection, and make the decision whether the correlation values of the matched filter outputs should be accumulated or be discarded by controlling the scrambling code coefficients. The channel estimator outputs the delay profile and early-late correlation magnitude for other functional blocks.

Besides the channel estimator, it contains a phase detector, initial phase setting block, initial frequency offset block, loop filter and a numerical control oscillator (NCO). The initial phase offset ϕ can be obtained by arctangent operation by I-channel correlation peak value(I_{s_pk}) and Q-channel correlation peak value(Q_{s_pk}) peak value of the significant path provided by channel estimator as shown:

$$\phi = \tan^{-1}\left[\frac{Q_{s\_pk}}{I_{s\_pk}}\right]. \tag{4}$$

The $\Delta\omega$ can be known by average phasor difference from consecutive two peak values. That is

$$\Delta\omega = \tan^{-1}\left[\frac{1}{k}\sum_{i=1}^{k}(I_{s\_pk,i} + Q_{s\_pk,i}) * (I_{s\_pk,(i+1)} + Q_{s\_pk,(i+1)})^*\right]. \tag{5}$$

In CDMA system, the sampling timing reflects on the alignment of the PN code. For that reason, the **d**elay-**l**ock **l**oop (DLL) [8]–[10] technique is one of most popular solutions for timing synchronization. In this proposed receiver, two kinds of timing synchronization have been implemented. First we adopt 4-time oversampling of the input data for coarse timing synchronization, which can provide the precision of 1/8 sampling clock. The other part is the proposed modified digital DLL for timing tracking. The block diagram of the timing recovery loop is shown as Fig. 3. The proposed timing recovery loop is composed of a interpolator, a loop filter, a NCO, and the early-late correlator included in the channel estimator.

The timing recovery loop starts to work when the channel estimator is in tracking mode since the information of the pilot symbol is output form channel estimator at symbol rate. The input data of the timing recovery loop is from the early-late correlator in the channel estimator.

D. Equalization and De-spreading

The rake receiver is most popular and conventional receiver in the DS-CDMA system. Unfortunately, the relative power density of delay spread of the HSDPA is quite large. This means that the receiver may encounter large ISI. At this scenario, the rake receiver can no longer provide satisfactory performance, so an equalizer should be adopted.

Fig. 4 is the block diagram of proposed adaptive LMS equalization and de-spreading architecture. This architecture consists of a random pattern generator, a 14-tapped length weight update filter, a 14-tapped length transversal filter and a correlator bank. The entire architecture can be separated into two operation modes: training mode and de-spreading mode.

In general, the training sequence is a random sequence with the properties close to the data symbol. The only one

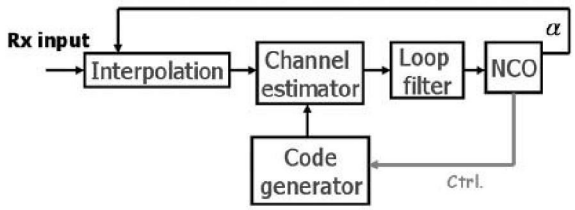

Fig. 3. Block diagram of timing synchronization.

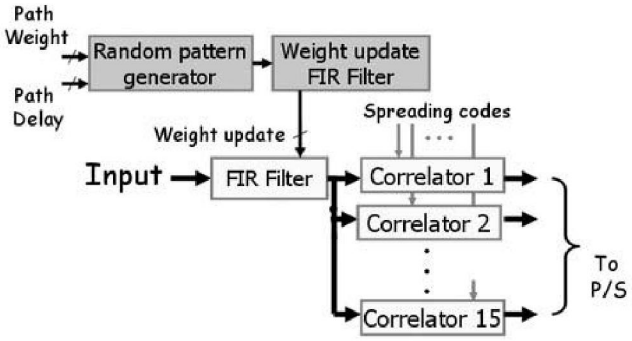

Fig. 4. Block diagram of equalization and de-spreading.

downlink physical channel with the known symbol pattern in this transceiver system is CPICH. However, the symbol pattern of this physical channel can not to be served as the training sequence because of its monotonous symbol pattern. In order to solve the problem of training sequence, we proposed the concept to generate the random training sequence by receiver itself. Because the training sequence is generated by receiver itself, thus it is necessary to join the channel conditions in training sequence for simulating the channel impulse response. In training mode of LMS algorithm, the training sequence which is used to training the weight update FIR filter. After finish training the weighting coefficients of update filter, the system will switch to de-spreading mode. In this mode, all functional blocks of entire architecture are under working. The filter of the input data symbol is working for eliminating the ISI effect with weighting factors from trained coefficients of the weight update filter. On the other hand, the random pattern generator and weight update FIR filter keeps updating the weight coefficients to data symbol filter periodically by monitoring the channel conditions to make equalization applicable in variable channel.

IV. System Simulation

A. System Performance Simulation

The floating point simulation results are used to evaluate system performance. The channel model adopted here is PB3 propagation condition of multi-path fading environment for HSDPA specified in 3GPP standard under 16-QAM. Moreover, 3-ppm carrier frequency offset and clock offset (6000 Hz relative to the 2GHz RF frequency and 15.36 MHz sample clock) are considered. The multi-code simulation is shown as Fig 5. Obviously, the maximum data rate of 10.8 Mbps can be achieved with satisfactory performance.

B. Fixed-point Simulation

The main objective of the fixed-point simulation is to figure out the minimum word length of the signals in receiver without critical system performance degradation. The fixed-point simulation performance approximates to floating-point simulation results.

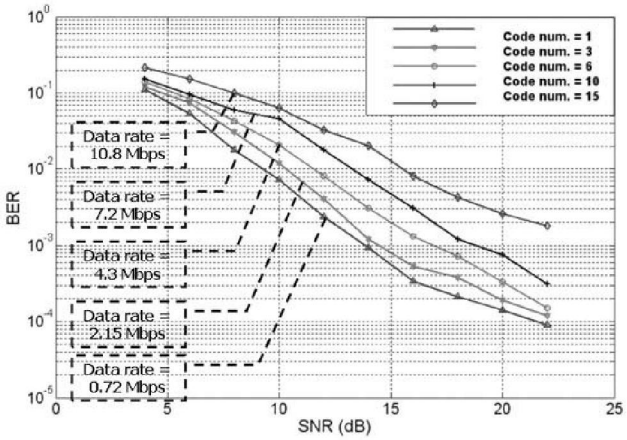

Fig. 5. BER versus SNR for multi-code simulation.

V. Architecture Analysis

As we known, the one of main factors occupies heavy area complexity and power dissipation in receiver is matched filter as shown in Fig. 6 in channel estimator and equalization circuit. Consider that, there are three main components of the matched filter: a tapped-delay-line, scrambling coders and Wallace tree adder. The tapped-delay-line is composed of the shift registers by D-type flip-flops for holding the incoming data. Since the complex scrambling code is bit operator, the operation can be accomplished by using two 4 to 1 multiplexers to select the product value. Besides, the Wallace tree adder with the 4:2 **c**arry-**s**ave **a**dder (CSA) is used for summing up the de-scrambling value. Therefore, hardware issues analysis can be done by these circuit components. In our hareware issues evaluation, several 1-bit operation units for 0.18-gm process at 1.8-V supply voltage are employed in complexity and power estimation.

The estimation results and comparisons of matched filters are shown in Table 2. Theoretically, by means of (1/4) symbol length matched filter can get 75% area and power reduction. Practically, there still need an additional logic control circuit block to execute the multiple-dwell algorithm we call PDSU previously. From Table 2, it is not hard to observe that the logic control circuit does not take much area and power. Therefore, by this algorithm, it still can achieve 50% area and power reduction as shown in Table2.

Besides matched filter, another component plays an important role of this baseband processor is LMS equalization. For convenience to analyze the dominant operation complexity of

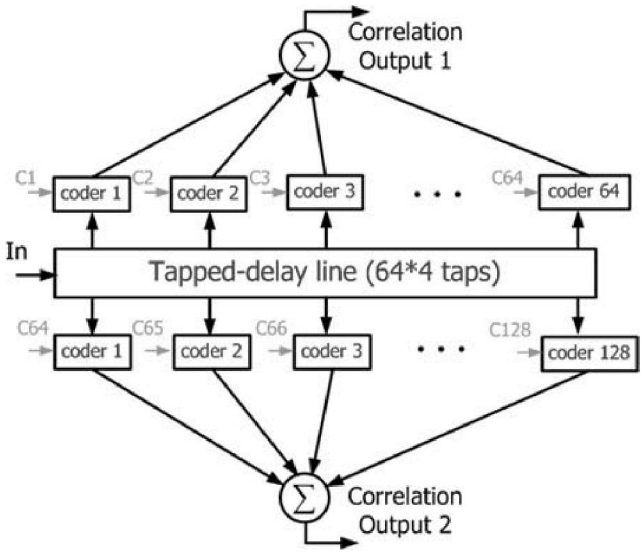

Fig. 6. Proposed matched filter architecture.

TABLE II
EVALUATION OF THE AREA AND POWER COMSUPTION OF MATCHED FILTER.

Estimation Items		1024 taps	This Work	Reduction Rate
Required Area (μm)^2	A_{Delay_line}	1351680	337920	75%
	$A_{Scrambling\_coder}$	1477632	738816	50%
	$A_{Wallace\_tree}$	534380	262920	51%
	$A_{Additional\_logical\_circuit}$	----------	289972	----------
	Total Area	3363692	1629628	51.6%
Power Consumption (mW)	P_{Delay_line}	2.45	0.612	75%
	$P_{Scrambling\_coder}$	5.05	2.525	50%
	$P_{Wallace\_tree}$	1.91	0.94	51%
	$P_{Additional\_logical\_circuit}$	----------	0.89	----------
	Total Power	9.41	4.967	47.2%
Normalized Area		1	0.484	
Normalized Power Consumption		1	0.528	

the equalization, a breakdown of this circuit component is shown in Table 3.

Evidently, the complex multiplications dominate the complexity. Needless to say, this part will consume much area and power in receiver if we implement it directly. It is necessary to replace these complex multipliers by means of advanced arithmetical algorithm circuits such as **CO**ordinate **R**otational **DI**gital **C**omputer (CORDIC) algorithm [11]or some other efficient implementations for complex multiplier.

VI. CONCLUSION

In this paper, system design, a baseband processor architecture for WCDMA/HSDPA communications is presented. In this system, the maximum data rate of 10.8 Mbps can be reached with 15 multi-code transmission. The proposed receiver consists of a channel estimator, a carrier synchronization, a timing synchronization and equalization. Because the

TABLE III
OPERATION BREAKDOWN OF PROPOSED EQUALIZATION.

		Number of Arithmetical Operation	Operating Frequency
Weight update IIR Filter	Complex Multiplication (14-bits)*(9-bits)	14	$f_{sampling}$
	Complex Addition 21-bits	14	$f_{sampling}$
Data IIR Filter	Complex Multiplication (15-bits)*(9-bits)	14	$f_{sampling}$
	Complex Addition 22-bits	14	$f_{sampling}$
LMS Updating	Complex Multiplication (15-bits)*(14-bits)	14	$f_{sampling}$
	Multiplication (16-bits)*(4*bits)	2	$f_{sampling}$
	Complex Addition 22-bits	14	$f_{sampling}$

higher modulation and some advanced transmission techniques have been adopted to achieve higher transmission data rate, the increasing of hardware complexity and power consumption is undoubtedly true. The multiple-dwell algorithm is adopted to design the complex matched filter in channel estimator. Via some preliminary analysis of matched filter and equalization, half of area complexity and power saving are expected of the proposed matched filter compared to a full-tap matched filter but still with satisfactory performance. Furthermore, advanced arithmetical algorithm and efficient implementations can be used to replace complex multipliers in equalization block to reduce implementation cost further.

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